

FIG.1

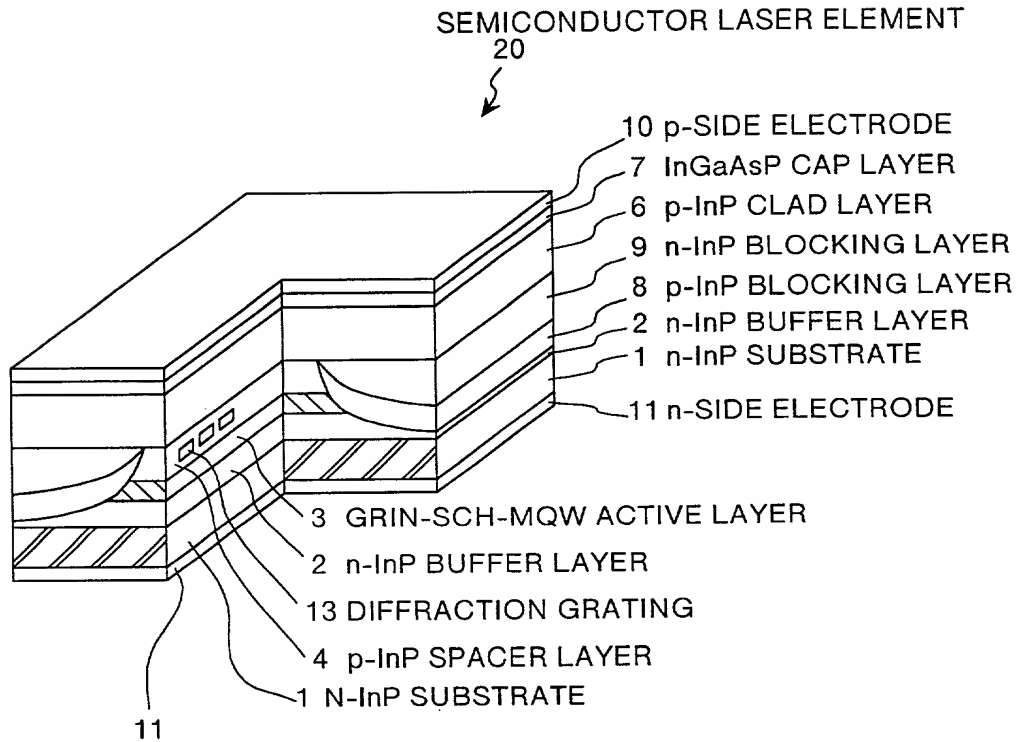


FIG.2

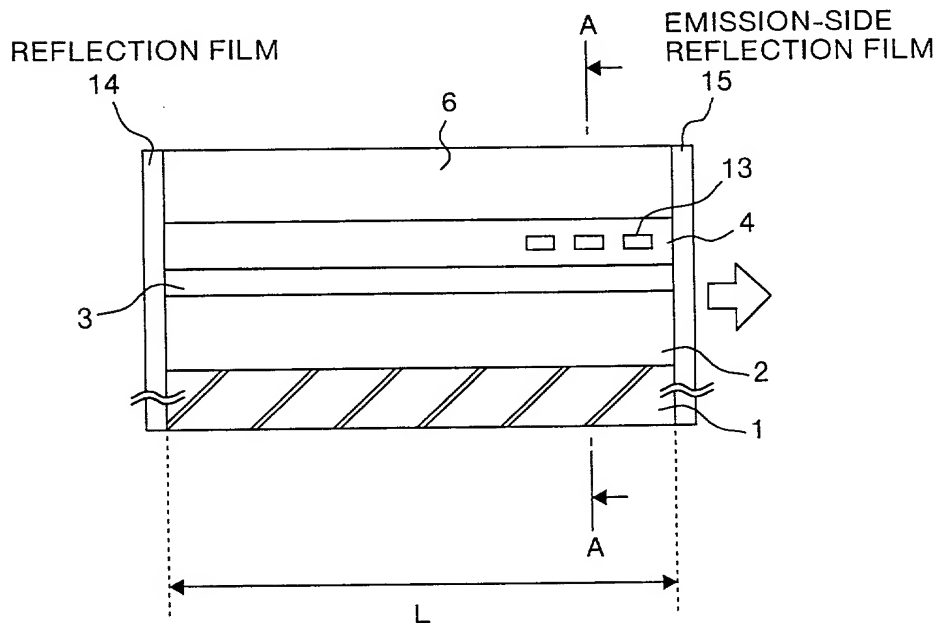


FIG.3

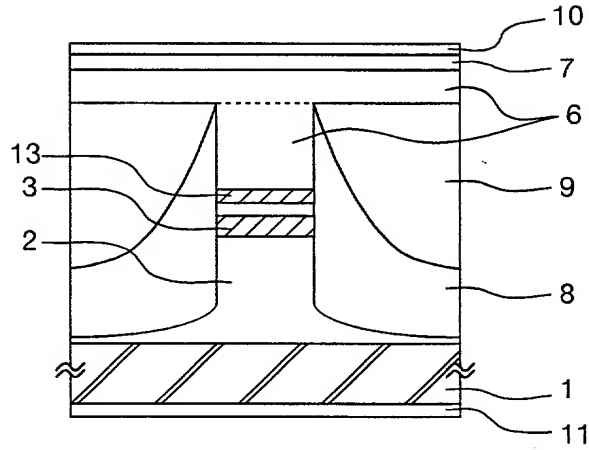


FIG.4

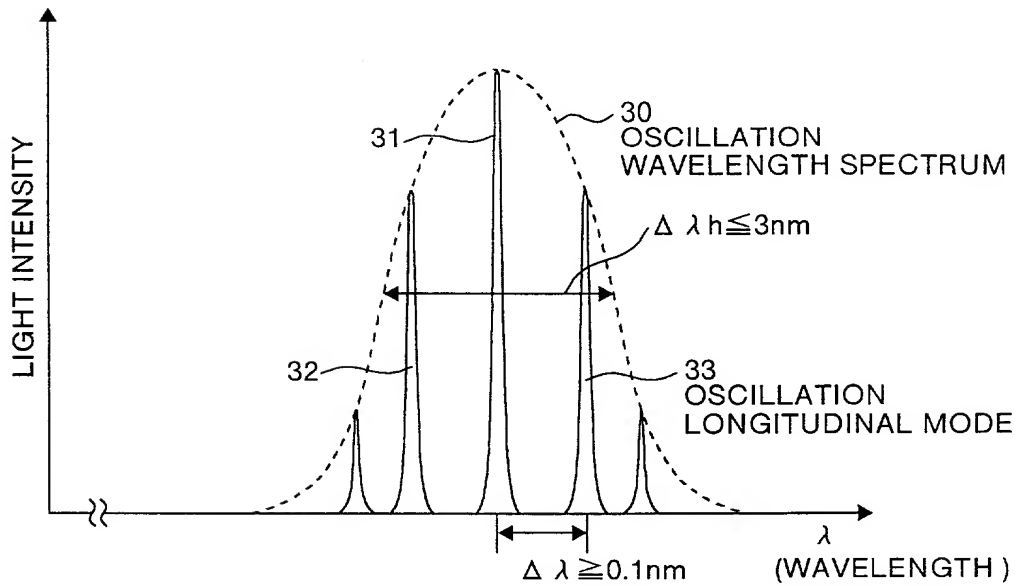




FIG. 6A

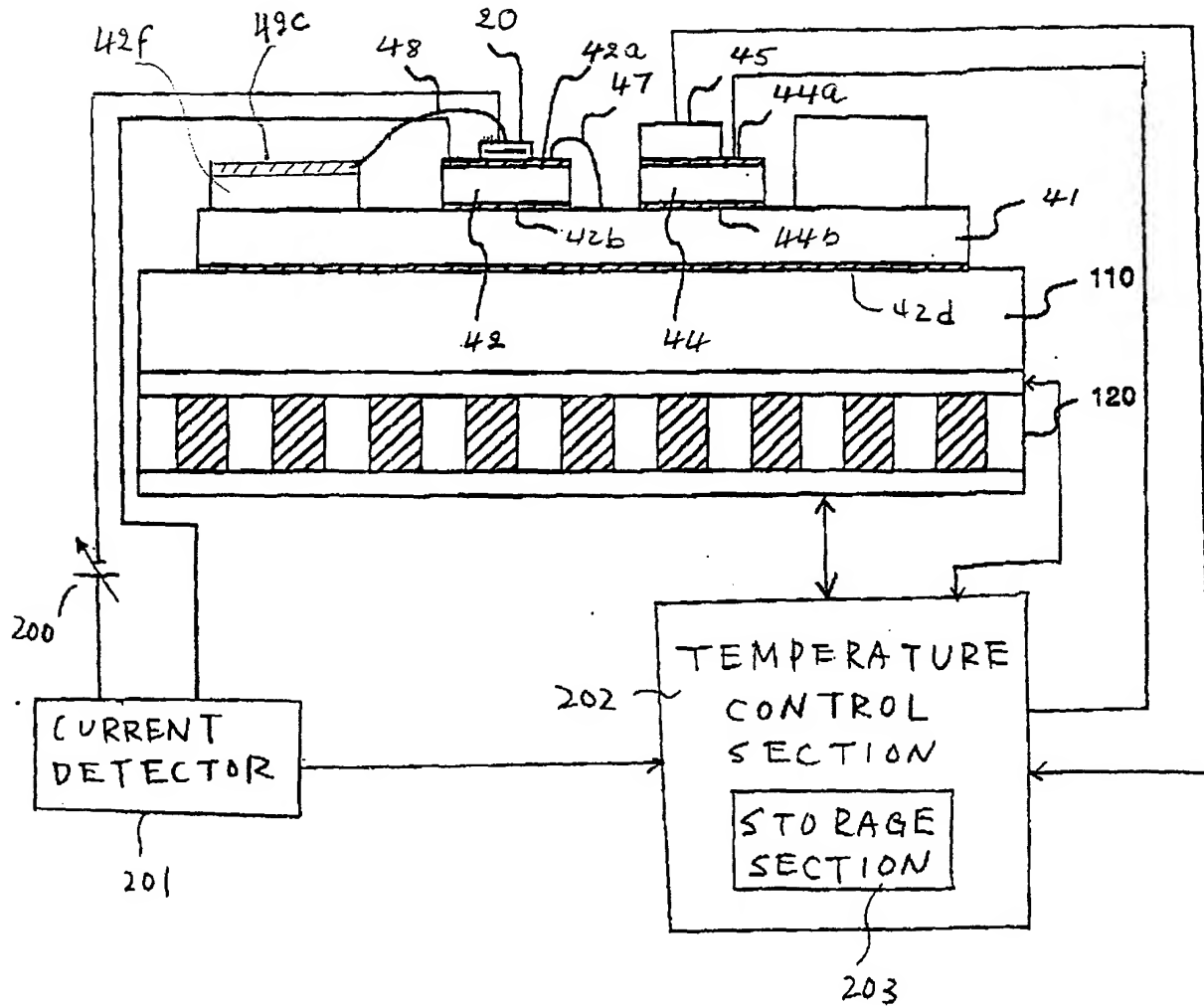
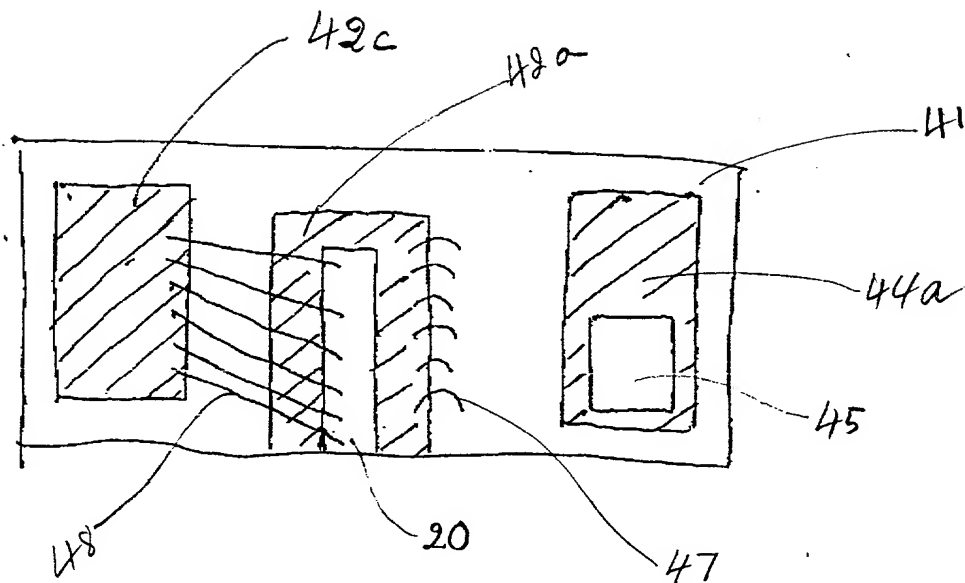


FIG. 6B



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FIG.7A

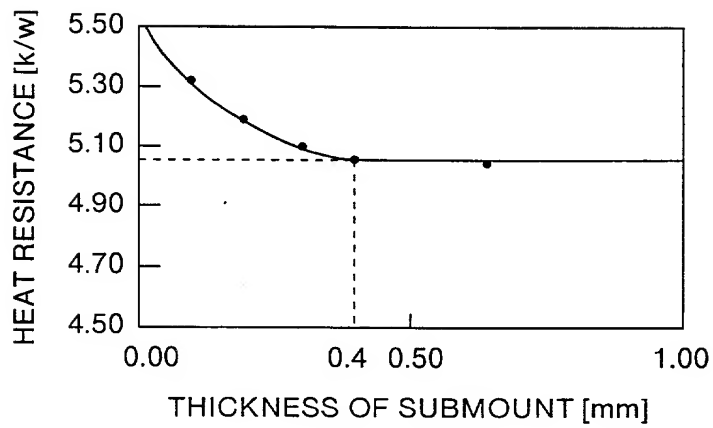


FIG.7B

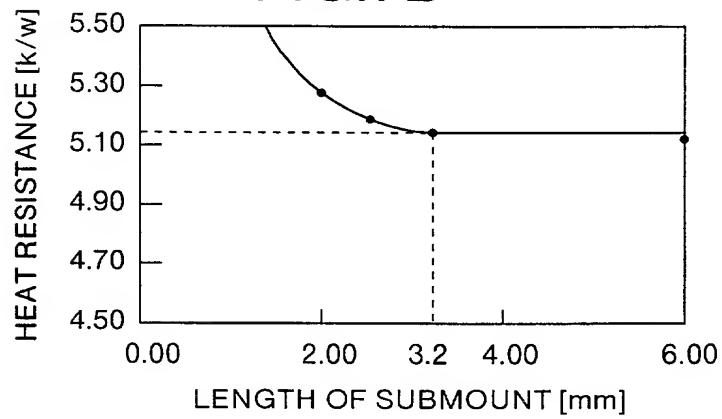
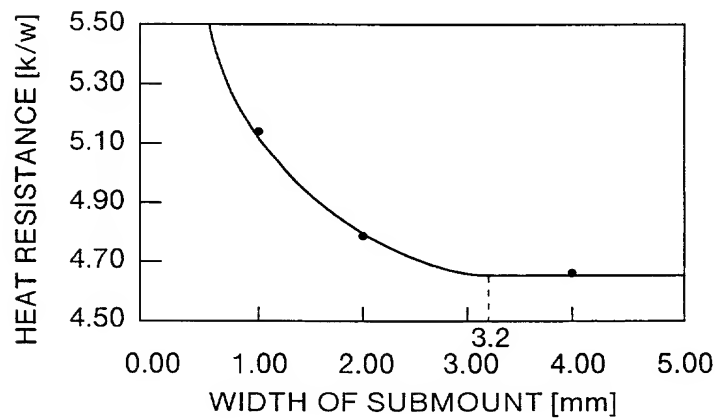


FIG.7C



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FIG.8

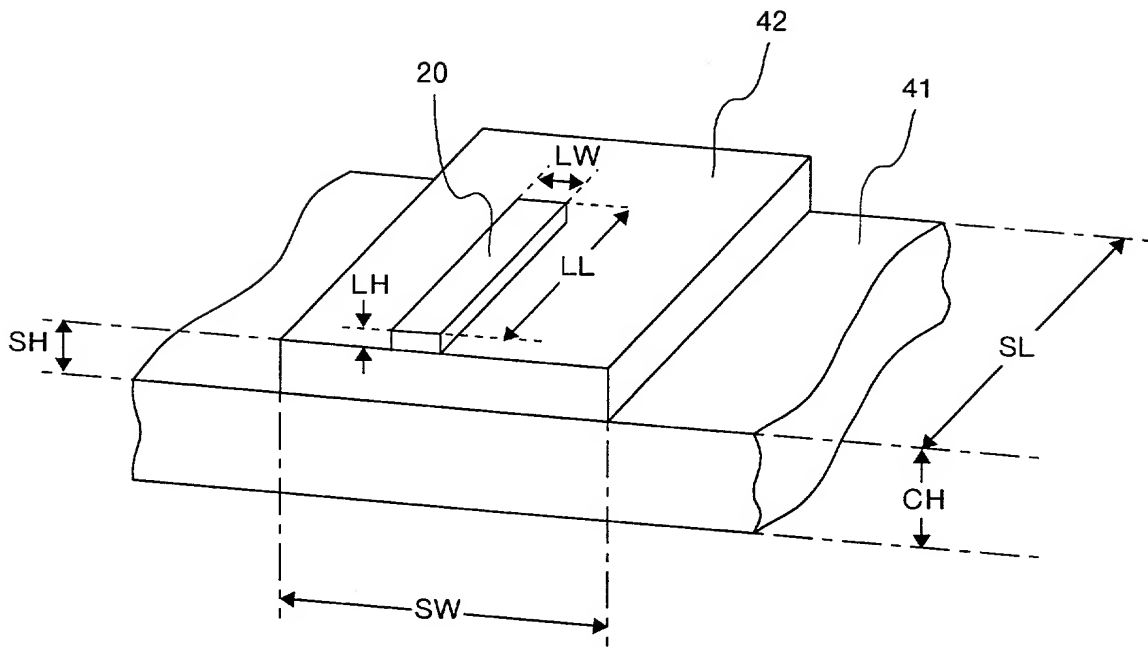


FIG. 8

FIG.9A

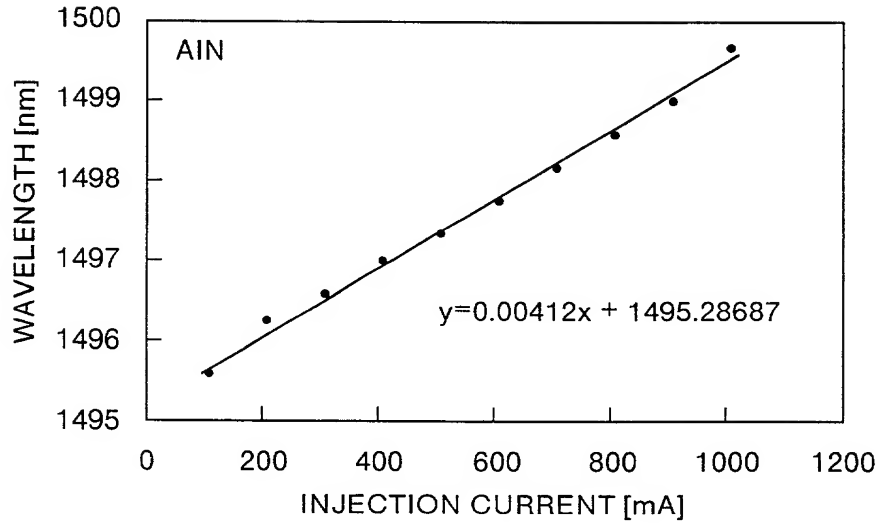


FIG.9B

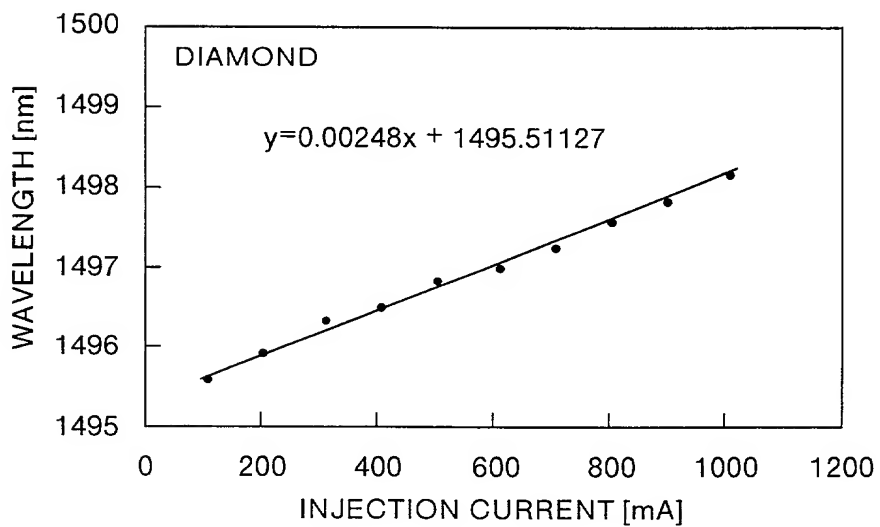




FIG.10

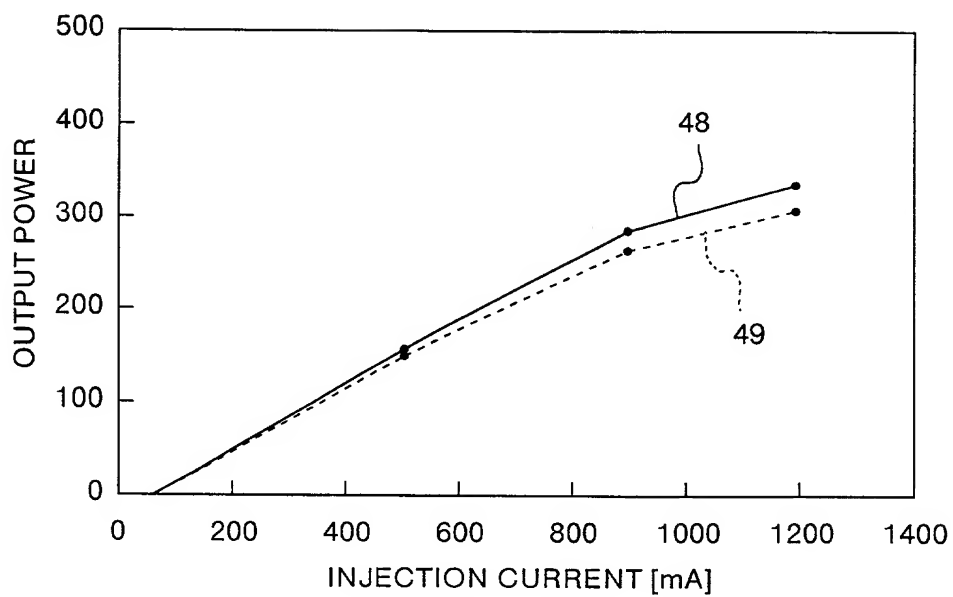


FIG.11

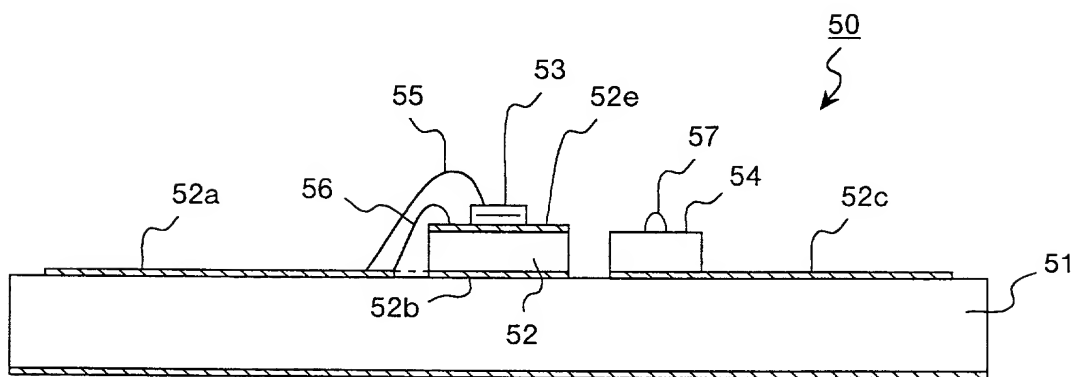


FIG.12A

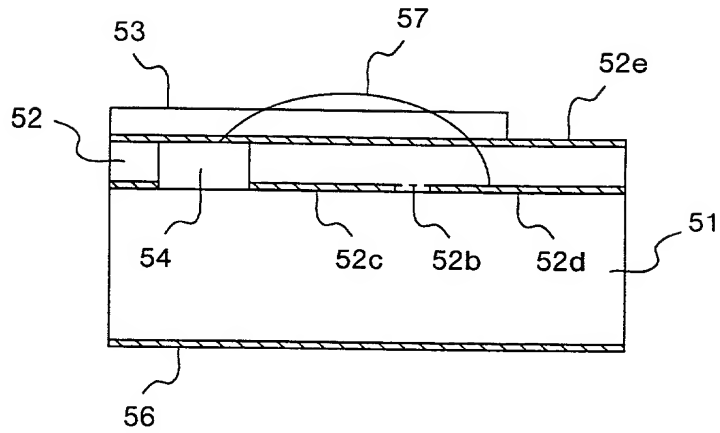


FIG.12B

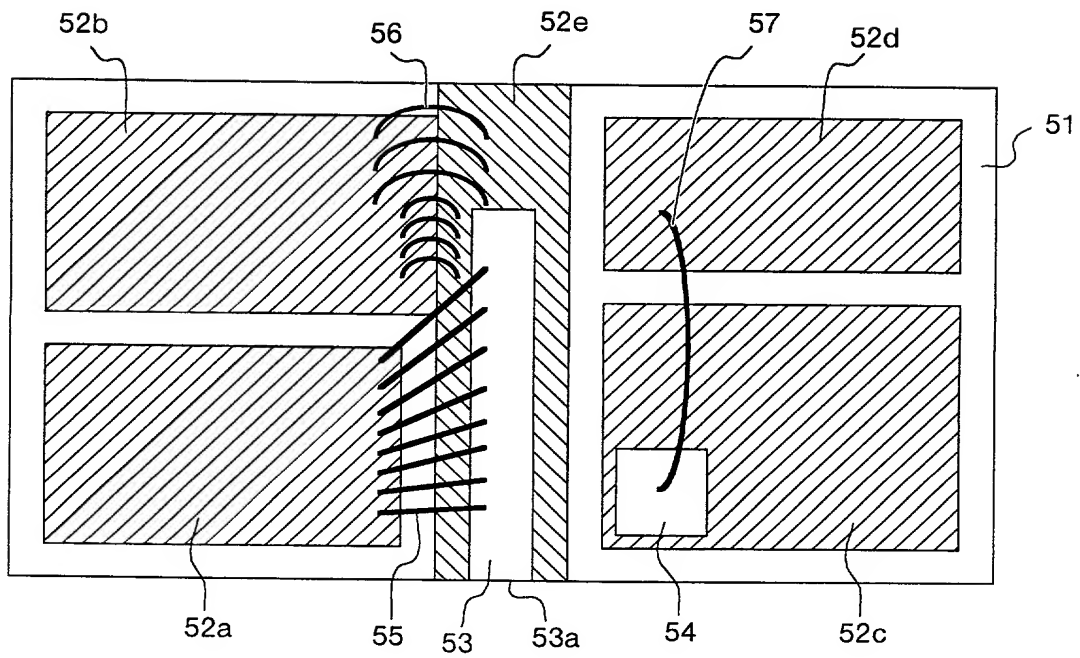


Figure 5 is a cross-sectional view of a semiconductor device 50'. The device includes a substrate 51, a thin layer 52, and various components including a gate 52a, a gate 52b, a gate 52c, a gate 52f, a gate 53, a gate 54, a gate 55, and a gate 57.

FIG.14A

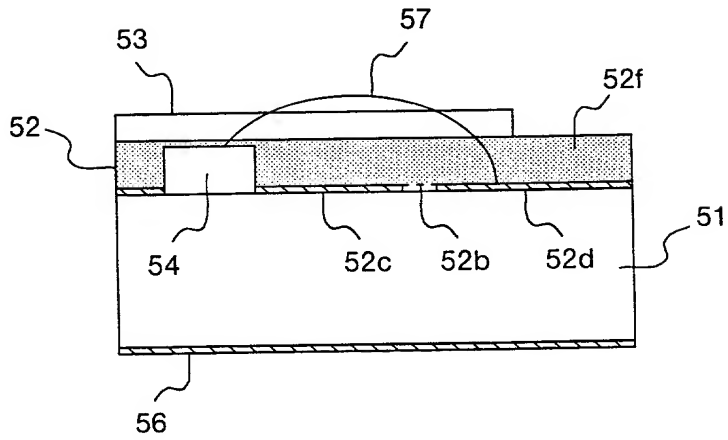


FIG.14B

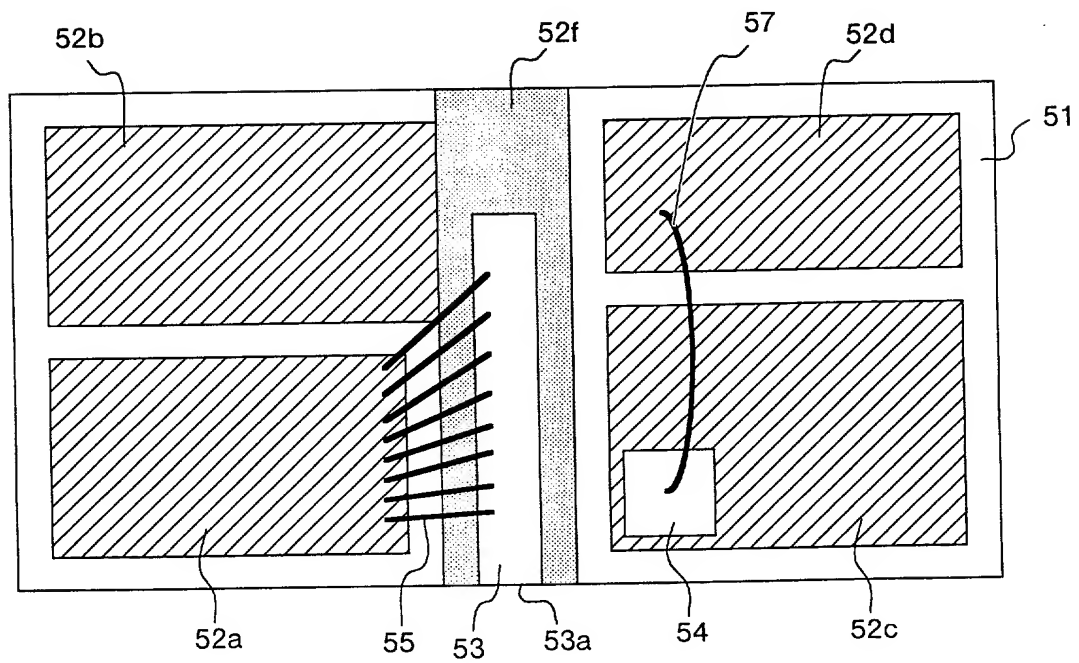


FIG. 15

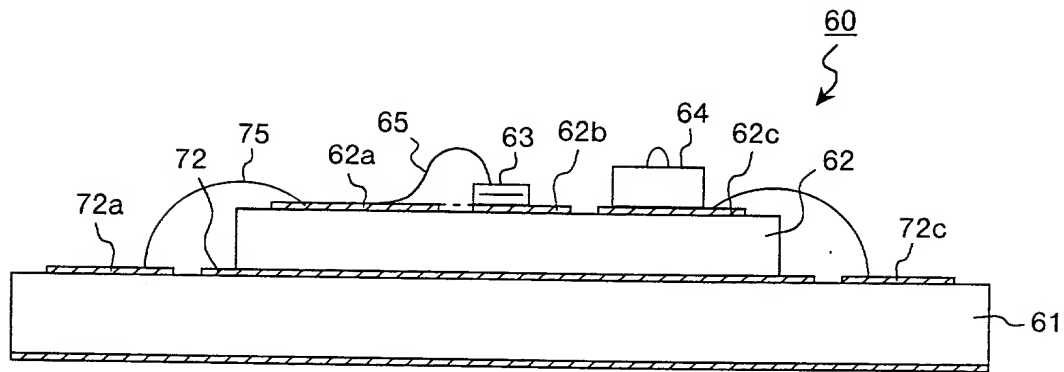


FIG.16A

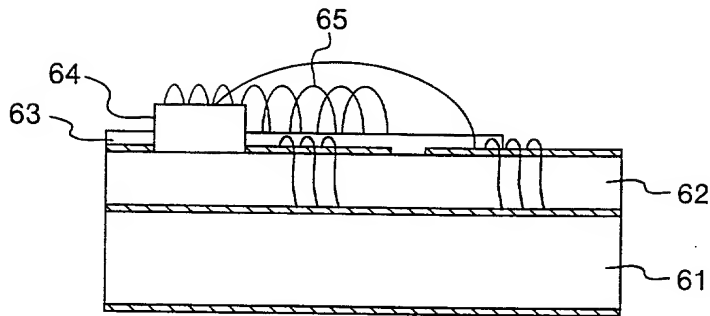


FIG.16B

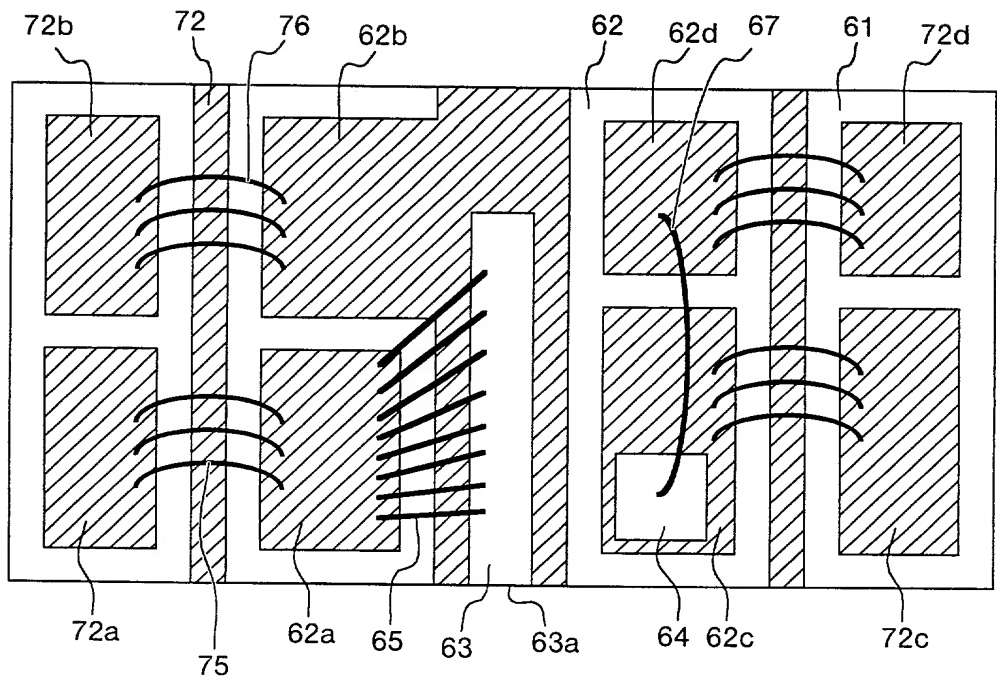
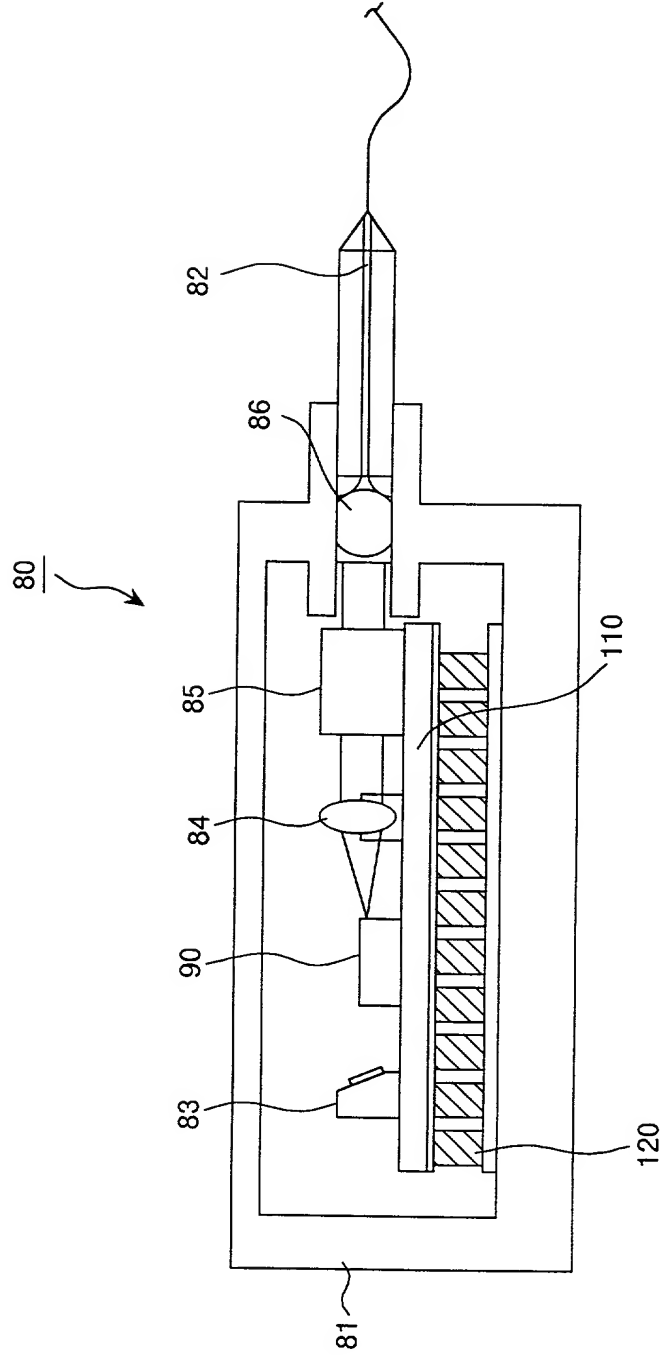


FIG.17



This cross-sectional view shows a substrate 110 with a patterned layer 102. A central structure 103 is formed on layer 102, consisting of a gate 105 and a contact 106a. A side structure 104a is also shown. The substrate is labeled 110 and 120.